Towards High-Level Models For Low-Power Systems

Florence Maraninchi
Computer Science, Joseph Fourier University, Grenoble

Abstract

We describe ongoing work on the modeling of energy consumption for systems in which the software has some control on the low-consumption modes of the various hardware devices (possibly with some feedback loop behavior). This includes systems-on-a-chip in objects like set-top-boxes, or sensor network nodes. We aim at defining a type of model intermediate between: (1) Detailed hardware emulators, on which the actual software can be run, but which can be quite slow; (2) Very abstract models in which the part of the model that represents the software is quite different from the actual software, and in which the hardware/software interface cannot be described (very common in the domain of sensor networks).
This means defining hardware models more abstract than full emulators, yet retaining the essential aspects of the hardware/software interface. Such models are intended to be used for early architecture exploration and design decisions, not for precise evaluations of energy consumption.
This work is based on the notion of transaction-level-modeling for systems-on-a-chip (TLM). We develop models in SystemC, or using the synchronous language Lustre developed at Verimag. With models in Lustre, we can benefit from all the validation tools of the Lustre toolbox (automatic testing, model-checking, abstract interpretation) and also from other tools like SMV. With models in SystemC, we mainly target efficient simulations, although some parallel work at Verimag addresses model-extraction from SystemC, to connect to verification tools.
This work is done in the context of several collaborative projects, with industrial partners. It is joint work with a number of colleagues and students at Verimag.

Biography

Florence Maraninchi received the Ph.D. in Computer Science and the "Habilitation a diriger des recherches (HDR)" from the University of Grenoble, France, in 1990 and 1997, respectively. In 1990, she joined UJF (Joseph Fourier University, Grenoble) as an assistant professor. In 2000, she joined Grenoble INP, where she currently holds a full professor position. From September 2005 to August 2007, she was with CNRS.
Her research activities are with the VERIMAG laboratory, where she is the head of the "synchrone" group. Her research interests include synchronous languages for embedded real-time components and systems, virtual prototyping of hardware-software systems (for functional properties and extra-functional properties like energy consumption),

modeling and validation of systems-on-a-chip at the transactional level (in cooperation with STmicroelectronics and DOCEA Power), modeling and analysis of ad-hoc sensor networks (in cooperation with FranceTelecom R&D and Coronis).
She teaches at ENSIMAG (the department of Computer Science, Applied Maths and Telecom of Grenoble INP). Her teaching interests include algorithms and programming languages, compiler design, formal verification of critical systems, basic circuit design, object-oriented modeling, formal models for time and parallelism, and embedded system design. She is in charge of the new Grenoble INP master programme on embedded software and systems. She is the co-author of two teaching books (in French): a book for beginners on algorithms and programming languages; a book for undergraduate students on the basics of circuits, computer organization and low level software.

http://www-verimag.imag.fr/
http://ensimag.grenoble-inp.fr/