Transaction Based Sequential Equivalence Checking of High Level Designs against RTL: Tips, Tricks, and Challenges

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Abstract

Hardware design at Electronic System Level (ESL) is becoming more mainstream, with larger and more complex blocks being pushed through the flow. Along with the move to higher level of abstraction, comes the ever increasing need for validation and verification. Formal sequential equivalence checking (SEC) is maturing along with the rest of the design tools for ESL. In this talk, I will present how SEC can be effectively applied to a few validation use cases in ESL flow, including golden model refinement, C v/s manually generated RTL, and High level synthesis (RTL). We will outline various axes along which SEC can be formulated for ESL designs, and what are the techniques and challenges for achieving formal proofs of sequential equivalence. In the talk, I will also briefly present SLEC, a family of formal sequential equivalence checking tools from Calypto.

Biography

Pankaj Chauhan is presently an architect of the SLEC product family at Calypto Design Systems in Santa Clara, California. He has contributed to various aspects of SLEC since Oct 2004, including sequential analysis engines such as induction, and model checking, word and bit-level solvers, word level netlist transformations and optimizations, abstractions and maps, optimization of SLEC usage for various use cases, etc.
He holds a bachelor in Computer Science and Engg. from the Indian Institute of Technology, Kharagpur, and a Masters and PhD in Computer Science from Carnegie Mellon University, Pittsburgh, Pennsylvania, USA.
His PhD thesis advisor was Prof. Edmund Clarke. His research interests are in increasing the capacity of formal verification engines through the use of abstractions, divide and conquer, SAT and SMT-BV solvers, and domain specific optimizations. Presently he enjoys watching trains, and visiting train stations with his 2 year old son.