Temperature-aware Test

Niraj K. Jha
Dept. of Electrical Engineering, Princeton University

Abstract

It is well known that during testing of a complex IC, power consumption can far exceed the values reached during its normal operation. High power consumption, combined with limited cooling support, leads to overheating of ICs. This can cause permanent damage to the chip or can invalidate test results due to changes in the path delay. Therefore, even good chips can fail the test. To prevent this problem, a methodology to generate the thermal profile of chips during test is needed. If such profiles are provided beforehand, temperature-aware testing techniques can be devised.

In this talk, we will present a methodology for thermally characterizing circuits under test. In this methodology, first, the test sequences for each targeted test strategy, namely, BIST, scan design and sequential test generation, are generated automatically. Then, power profiles are extracted by using the switching activity information obtained from simulations. Finally, a very fast thermal profiling tool is used to produce the final thermal profiles. Such a thermal characterization can be leveraged for temperature-aware system-level test scheduling. Results demonstrate that low power testing techniques are not necessarily temperature-aware. Thus, a concerted effort is necessary for developing temperature-aware test techniques.

We will then move on to the test challenges posed by double-gate CMOS technology, such as FinFETs, which are expected to bridge the gap to the 10nm technology node as single-gate CMOS runs out of steam. Temperature-aware test will be even more important for FinFETs.

Biography

Niraj K. Jha received his B.Tech. degree in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur, India in 1981 and Ph.D. degree in Electrical Engineering from University of Illinois at Urbana-Champaign in 1985. He is a Professor of Electrical Engineering at Princeton University. He is a Fellow of IEEE and ACM. He has co-authored four books, including a textbook titled ``Testing of Digital Systems" and the 3rd edition of ``Switching and Finite Automata Theory," and 350 papers. He is the editor-in-chief of IEEE Trans. on VLSI Systems and serves or has served

on the editorial boards of several other journals, such as IEEE Trans. on CAD, IEEE Trans. on Circuits and Systems I & II, Journal of Electronic Testing: Theory and Applications, and Journal of Low Power Electronics. He has co-authored 13 papers that have won various awards. His research interests include digital system testing, nanotechnology, embedded system analysis and design, power/thermal-aware hardware/software design, computer-aided design of ICs and systems, computer architecture, and computer security.