The challenges of Power estimation and Power-silicon correlation

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Acknowledgements

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Agenda

- Introduction
- Can we predict power accurately?
- Short Circuit power
- Leakage
- Estimation vs. silicon
- Summary
Introduction

Power is the #1 limiter of Moore’s law

• Heat-sinks cannot cool more than ~130W
• Systems: limitations of heat dissipation & power consumption
  – Servers, desk tops, small form factor, lap-tops
  – Most systems allow much less than 130W
• Battery life for portable devices
• Leakage power - a significant component in deep sub-micron
  – 20-50% of the overall power at active mode
  – Dominates battery time in many usage scenarios
Design for low power

Requires same concepts as design for high frequency

- Power budgets
- Power estimation and analysis
- Power-performance optimization
- Validation/rollup

Accurate power estimation and good power-Si correlation are keys for low power design
How to estimate power

Simplistic power model
- \( P = C V^2 f \) AF
- AF is estimated by some high power test
- Leakage is roughly liner with total \( Z / \) device count

This is indeed simplistic!
- C is not that simple
  - Voltage dependent; Xcap (Miller effect)
- AF is not straight forward
  - Proper work loads; Glitches
- Additional power components
  - Short circuit, contention
- Leakage is sensitive to everything
  - In particular process, temperature, and voltage variations
- Full blown circuit simulation is far too slow
  - Also useless until the design is mature enough
  - And, still not fully accurate due to Xcap and process variations
Can we predict power accurately?

Power model: \[ P_{\text{tot}} = P_{\text{lkg}} + P_{\text{dyn}} = P_{\text{lkg}} + P_{\text{sw}} + P_{\text{sc}} + P_{\text{cont}} + P_{\text{glitch}} \]

Simulation based “model” on inverters chain
- 8% gap between min and max C
- AF, SP, leakage, and SC are directly measured
- Using max-C result in 3% over-estimation

Power estimation is far harder when applied to Full Chip
- Circuit includes more gates than just inverters
- C is estimated by (static) RC extract tools
- SC depends on slopes; timing only provides min/max slopes
- Contentions and glitches are hard to predict and model
- Analog & special circuits require special handling
- Leakage is sensitive to within-die and die-to-die variations
**Power components “model” vs. simulation**

**Simulation:**
“Model” is based on simulated inverters chain and “measurements”
- AF = 1
- Cap, Xcap
- SC directly measured

**Accuracy:** ~3%

**Real life:**
Not only inverters
C from RC-ext.
Xcap estimated
AF/SP by logic sim.
SC estimated
Contention
Glitches

**Accuracy:** ???

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**Switching power: min and max cap (P1264)**

- Gap = 8%

**Total Heat Dissipation (1264)**

- Gap = 3%

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**Power components**

- SW
- Lkg
- SC

**Total based on Cmax & MCF=4**

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**Sort-circuit / Switching Power (%)**
Why Xcap/Miller consumes more power

Regular capacitor:

\[ \text{Power} = C V_{cc}^2 f AF \]

Voltage swing = \( V_{cc} \)

Xcap

\[ \text{Power} = 4 C V_{cc}^2 f AF \]

Voltage swing = \( 2V_{cc} \)

Xcap/Miller cap consumes **4X** the power of regular capacitor.

De-coupling only provides a factor of 2.

Impact: gate-drain (Miller); IC Xcap
Sensitivity to irregular waveform

Example: marginal set-up time on a latch

- Waveform within the latch becomes very irregular
- Causes huge SC on the inverter that drives the output pin and on its receiver (not shown)

Bad waveforms / long tails are expected on weak drivers like min-delay buffers and drivers that are down-sized to save power 😞
Short circuit Power - a simple model

Model: unloaded symmetric inverter

Current is dominated by device in saturation, $V_{ds} > V_{gs} - V_{t} > 0$

Simple MOS model, $I_{dsat} = K/2 \ (V_{gs} - V_{t})^{2}$

$AF=1$ (2 transitions per cycle), current is symmetric around $V_{in} = V_{cc}/2$

Clock period = $T$, slope = $\tau$

$$I_{av} = 2 \frac{2}{T} \int_{t_{1}}^{t_{2}} \frac{K}{2} (V_{in} - V_{t})^{2} \, dt$$

$$V_{in} = \frac{t - t_{1}}{\tau} V_{cc} \ ; \ \frac{dV_{in}}{dt} = \frac{V_{cc}}{\tau} \ dt$$

$$I_{av} = 2 \frac{2}{T} \int_{V_{i}}^{V_{cc}/2} \frac{K}{2} (V_{in} - V_{t})^{2} \frac{\tau}{V_{cc}} \, dV_{in} = \frac{K}{12} \frac{\tau}{T} \frac{1}{V_{cc}} \left(V_{cc} - 2V_{t}\right)^{3}$$

$$P_{sc} = I_{av} V_{cc} = \frac{K}{12} \frac{\tau}{T} \left(V_{cc} - 2V_{t}\right)^{3}$$

Short circuit model – cont.

Some re-ordering:

\[ P_{sc} = \frac{K}{12} T_f f(V_{cc} - 2V_T)^3 \]
\[ = \alpha \{ V_{cc}^3 - (6V_T)V_{cc}^2 + (12V_T^2)V_{cc} - 8V_T^3 \} \]
\[ = aV_{cc}^3 - bV_{cc}^2 + cV_{cc} - d \]

Curve fit enables 3 independent Vt estimates:

\[ V_T = \frac{b}{6a} ; \frac{c}{2b} ; \frac{3d}{2c} \]

- It also predicts cube dependency in Vt
- SC(T) should be explained by Vt(T)

Is it applicable for deep sub-micron devices?
Possibly – integral quantity might not be very sensitive to details
SC simulations & Fit to theory

**SC vs. Vcc**

1264 step B

**SC vs. Vt**

1264 step A

Vt (normalized):

b/6a = 1.000

c/2b = 1.017

3d/2c = 1.012
SC model versus simulation

Simulations indicate that the model is applicable for deep sub-micron devices

- Results were fitted to a 3rd order polynomial
  - No restrictions on the coefficients a, b, c, d
- All 3 ratios result in almost identical Vt value
  - And the resulted Vt fits the process Vt
- SC power also fits a 3rd order polynomial in Vt
- The temperature dependence of the SC power is is fully explained by Vt(T)

So now let’s compare with Si data
Cdyn with SC correction

\[ C_{dyn} = C_{pure} + C_{rt} \frac{(V_{cc} - 2V_{t})^3}{V_{cc}^2} \]
\[ V_{t} (SICC, T) = V_{t} - dV_{t}SICC \times SICC - dV_{t}T \times T \]

Conclusion: SC model fits Si very well

- Cdyn becomes V, T, SICC independent
- Enables extracting SC power from Si measurements
Modeling Leakage

Die to die and within die variations

- +/- 20% frequency var.
- >10X leakage variations

Si measurements require a very large amount of dies

DC simulations are insufficient to estimate leakage

(Ref: Pat Gelsinger, keynotes DAC 2004)
Estimates vs. Silicon

Power - Si correlation

• Comparing FC power vs. silicon, no finer granularity!

We need richer power measurements and analysis methods

• Separate dynamic and leakage Power
  – Not a trivial task! \( P_{\text{dyn}} \neq P_{\text{tot}} - Vcc \times SICC \)
  – Requires thermal maps and a proper model

• Measure power as function of \( Vcc, f, T, \) fast/slow dies

• Power measurements & estimates at different work loads

• Fine spatial resolution measurements
  – IREM is a partial solution
  – Possibly built-in probes for leakage and for dynamic power
Summary

Power is one of the major challenges of the VLSI and SoC community

Power is far more complex than $C V^2 f A F$

Poor abilities to correlate Power estimates with Si

Room for further research on power modeling and on power-Si correlation at product level