Department of Electrical Engineering

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IRWIN AND JOAN JACOBS
CENTER FOR COMMUNICATION AND
INFORMATION TECHNOLOGIES (CCIT)

IEEE

IEEE / ACRC Workshop

on

Memristors and Resistive Memory Devices and Applications in Computer Architecture and Brain-Inspired Systems

Date: **Wednesday, March 7, 2012**

Location: **Technion, EE building, Auditorium 280 (2nd floor)**

Goal: **Novel devices, based on reversible changes in electrical resistance, are emerging as potential solutions to problems in digital electronics. These devices also hold promise as key elements in future brain-like hardware systems.**
The goal of this workshop is to introduce researchers and developers from diverse communities (physics, engineering, brain research, industry) to this new field.

Agenda:

09:00 - 09:30 Registration and refreshments

09:30 - 10:35 ***Session 1*** ***Opening and Keynote***

Prof. Adam Shwartz **Welcome and opening remarks**

Prof. Sung-Mo Kang (University of California)

Keynote: Memristors and Their Applications to Nanocomputing

As memory and computing technologies rapidly advance to increase integration density for more complex information processing, CMOS technologies encounter increasingly higher physical limitations in lithography, process variations control and power density. The imminent barriers to Moore's Law call for disruptive idea of VLSI building blocks for next generation electronics. Responsive efforts span from investigation of new physical state variables other than charge or voltage to novel nanoelectronic devices and circuit architectures offering ultra-dense memory, and low-power logic and reconfigurable hardware architectures Memristors were first conjectured based on the missing constitutive link between flux and charge by Leon Chua as published in his seminal paper in 1971, which was further extended by L. O. Chua and S. M. Kang in their 1976 paper on memristive devices and systems. Recently physical realization of memristors was reported in Nature by HP's Stan Williams team in 2008. Memristors offer nonvolatile resistance as a state variable. Nanoscale memristors can be configured for NVRAM memories, logic gates, reconfigurable interconnects and nonvolatile latches with high integration density and, more importantly, with CMOS compatibility, the NVRAM technology together with CMOS has become a leading technology. Many interesting memristor realizations and applications in analog circuits, digital circuits, neuromorphic circuits, RRAM, CAM, and FPGAs and others have been reported in many literatures and international meetings. In this talk we will examine the unique features and applications of memristors that can contribute to 3D integration and nanocomputing with high packing density and reduced power consumption.

10:35 - 10:45 Break

10:45 - 12:00 ***Session 2*** ***Material Properties and Device Physics***

Prof. Ilan Riess (Technion)

Devices based on Mixed Ionic Electronic Condutors (MIEC)

We discuss switching devices where the resistance changes due to stoichiometry changes. For that, point defects, stoichiometry change, ionic current and ambipolar diffusion of ions and electrons or holes are called upon. Reference is made specifically to oxides where the ionic defects are oxygen vacancies. They act as native donors. The motion of ionic defects under an applied voltage results in dramatic changes in the electron/hole current leading to hysteresis and quasi switching under certain condition and under others may also lead to switching and in addition to memory. Different options for achieving memory are discussed and compared to those used in flash memory and in phase change memory devices. The role of nonlinear I-V relations for switching as well as for memory is emphasized. A preferred design that we are working on is presented. Writing, both on and off, involves ionic current. Loss of memory is by ambipolar motion. The significance of a pulse for writing and current compliance are emphasized. Theoretical results and experimental partial results supporting our view of this kind of memristors are presented.

Eilam Yalon (Technion)

Resistive Switching Probed by a Metal-Insulator- Semiconductor Bipolar Transistor

Resistive switching in thin dielectric films is studied using a metal-insulator-semiconductor bipolar transistor structure. Using this structure, electron injection into the semiconductor valence band can be distinguished from injection into the conduction band. In

addition, the p-n junction serves as a sensitive detector of damage induced by the switching effect. In this talk I will discuss the implications of the obtained experimental results on the validity of various conduction mechanisms through the insulator.

Dr. Nuriel Amir (KLA)

Phase-Change Memory

Phase-change memory is one of the most mature types of memristors, almost reaching commercial status. The material most commonly used for PCM is a Chalcogenide alloy called GST (GeSbTe) with a crystalline conductive state and an amorphous high resistive state. Chalcogenide is also used for DVD-RW. One of the main advantages of PCM is its scalability. In this talk the principles of PCM operation and the reasons it scales well will be discussed. Recent progress on making a PCM Switch (PCMS) will be described, as well as multi bit per cell.

12:00 - 13:15 ***Session 3*** ***Circuits***

Dr. Yakov Roizin (Tower Semiconductor)

Resistive Memories Promising for Industrial Applications

The interest of semiconductor industry to resistive RAM has been increasing, expecting a storage class memory that combines large capacity, high endurance and high switching speed. Several known semiconductor companies developed products or demonstrated ReRAM prototypes. The talk focuses on emerging ReRAM solutions employing CMOS fab compatible materials and technologies. Corresponding memory cells, array organization and switching mechanisms are reviewed. The discussed memories are compared with other novel NVM solutions, in particular currently developed by TowerJazz together with Crocus Technologies thermally assisted MRAM technology. Phase change memories and memristor approaches are mentioned in brief, assuming their detailed coverage in dedicated talks.

Prof. Eby Friedman (U. Rochester)

Spin Torque MTJ-Based Circuits for VLSI Applications

High performance microprocessors and systems-on-chip have long been constrained by limited memory and bandwidth. Traditional on-chip memory is affected by degraded cell stability with each subsequent technology node as well as growing leakage current. Moreover, the explosion of on-chip cores has resulted in higher requirements for on-chip bandwidth. Memristive circuits provide enhanced functionality that can be leveraged in existing applications to meliorate these growing issues. This talk will highlight some early research involving memory and interconnect design that leverages memristors for adata storage, on-chip memory, and high bandwidth interconnects.

Shahar Kvatinsky (Technion)

Memristor-based Logic Circuit Design

Memristors are novel devices which can be used in applications such as memory, analog circuits, neuromorphic systems, as well as logic gates. This talk is focused on logic design with memristors. In this talk several memristor-based logic families are introduced – IMPLY logic gate, MAGIC (Memristor Aided Logic), memristor-based PLA, and hybrid memristor-CMOS logic gates. Design considerations for memristor-based logic design are discussed, as well as the computer architecture insights for the use of memristors as logic gates in addition to memory.

13:15 – 14:00 Lunch break

14:00 – 15:30 ***Session 4*** ***Applications in Brain-Inspired Systems***

Prof. Naftali (Tali) Tishby (Hebrew University)

Some architecture inspirations from the biological brain

	Prof. Shimon Marom (Technion)	**Applying Memristors: Lessons from Biology** **There is a practical identity between memristors and a major class of functional proteins in biology: ionic channels. These proteins stand at the basis of intertwined memory and information transmitting processes in biological cells in general, and in electrically excitable tissues (notably the brain and the heart) in particular. I will briefly relate to the biophysics of ionic channels, and explain how biology makes use of these memristic proteins to (1) temporally integrate and store past input statistics, and (2) adaptively modulate the connectivity in neural networks. While hopes for applicable, biologically-flavored, memristor-based devices will be expressed, caveats of over-biologizing will also be stressed.**
	Alon Ascoli (Politecnico di Torino)	**Influence of memristor synapses on neuron-to-neuron interactions** **Biological systems use synchronization mechanisms to communicate. Employing mathematical models to describe a simple network of two memristor-coupled neurons, it is shown that memristor dynamics strongly affect the communication between the neurons.**
	Rafi Gidron (Israel BrainTechnology)	**Brain Inspired Computing** **The physical limits of conventional computer designs are within sight as nanoscale circuits cannot shrink much further. Power consumption of current computing technology also limits the growing computing capacity requirements that are driven by new digital data from sensors, online commerce, social networks, video streams and corporate and government databases.To meet the challenge, a different computation architecture approach will be needed. And brain inspired computing or neuromorphic computing might offers a potential solution path. The talk will review the opportunity as well as recent discoveries and research activities in the field.**
15:30 - 15: 45		Coffee Break
15:45 –17:00	***Session 5***	***Applications in Computer Architecture***
	Avi Klein (Sandisk)	**Emerging Memory Technologies: Applications** **In this session we will review the NAND Flash scaling limitations and the need to continue NVM cost reduction following Moore's Law. Several of the emerging memory technologies capabilities will be compared, with focus on ReRAM. We will then review the market application trends and what memory specifications are needed for these applications. We will summarize the presentation with the challenges ahead of ReRAM to meet these requirements.**
	Prof. Uri Weiser (Technion)	**Memory Intensive Architectures** **Logical separation between memory and CPU has been a basic principle for modeling and building computers. In recent technology generations, this principle caused physical separation between memories and computing elements, which has become the limiter due to interconnect power inefficiency. Future memory technology should cause a new architectural thinking in which memory and logic intermingle to provide a better product characteristics (e.g. performance, throughput, energy efficiency under the constrains (e.g. power, energy).** **The new future memory technology may initiate the next step function in Computer Architecture.**

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