Software-Defined Everything: High-level design and validation

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Abstract

We are in the middle of a major shift in product architectures - one in which many more processors are being used to deliver optimal, flexible product functionality. Previous product generations in many domains that used simple control processors and a host of RTL blocks are moving to increase the use of Application-Specific Instruction set Processors (ASIPs), configurable and extensible ASIPs, DSPs and application-specific controllers in a wide variety of architectures. This product architecture change is by no means complete, but we can see the rise of SDE - "Software-Defined Everything" occurring. This shift complements the increasing use of complex SoC devices and the continued expansion in use of reusable IP blocks from external and internal suppliers.

As a result of this shift design and verification processes, tools and methods must change, and are changing. Increased use of SDE has made Electronic System Level (ESL) design and validation tools and methods not just a desirability, but a necessity, from early architectural definition through to whole-design validation. Processor-based SDE design has its own particular verification and validation approaches - previous methods used with HW-centric design do not scale to the new world. Methodologies and tools must move quickly to this new approach.

In this talk, I will talk about the shift in design architectures, illustrated by examples, and the shift to new design approaches. I will discuss what changes in the move to new higher-level design and validation has worked and what has not. I will also discuss key areas for tool and methodology development in the future. All of this will be based on a pragmatic analysis of where industry has been, is currently, and where it is going.

Biography

Grant Martin is a Chief Scientist at Tensilica, Inc. in Santa Clara, California.
Before that, Grant worked for Burroughs in Scotland for 6 years; Nortel/BNR in Canada for 10 years; and Cadence Design Systems for 9 years, eventually becoming a Cadence Fellow in their Labs. He received his Bachelor's and Master's degrees in Mathematics (Combinatorics and Optimisation) from the University of Waterloo, Canada, in 1977 and

1978.
Grant is a co-author or co-editor of ten books dealing with SoC design, SystemC, UML, modelling, EDA for integrated circuits and system-level design, including the first book on SoC design published in Russian. His most recent book, "ESL Models and their Application: Electronic System Level Design and Verification in Practice", written with Brian Bailey, was published by Springer in January, 2010. He is a co-editor of the Springer Embedded Systems Series.
He was co-chair of the DAC Technical Programme Committee for Methods for 2005 and 2006.
His particular areas of interest include IP-based design of system-on-chip, platform-based design, and baseband processing.
Grant is a Senior Member of the IEEE.